Speeding Development of an FPGA-based Medical Device Using a Hardware Simulator

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NI Products Used:
sbRIO9636
LabVIEW 2012

Category:
Machine Control

The Challenge

Quickly develop reliable code for a medical device with multiple digital and analog inputs prior to having the hardware in hand for testing.

The Solution

We designed a hardware simulation board with voltage bridges and switches to simulate the behavior of the actual hardware, and coupled it with an application running in parallel with the primary code to report the actual values measured by the sbRIO.

Background

Data Science Automation (DSA) is a premier National Instruments (NI) Alliance Partner that specializes in automating and educating the world leading companies. Clients choose DSA because of DSA's deep knowledge of National Instruments products, disciplined process of developing adaptive project solutions, staff of skilled Certified LabVIEW Architects and Certified Professional Instructors, and unique focus on empowerment through education and co-development.

DSA won a major contract to develop the software for a sophisticated medical treatment system that takes the blood from a patient, removes unwanted components, and returns the purified blood to the patient over the course of several hours. Because of the importance of patient safety, the system is being developed with stringent testing protocols in place. For rapid development, LabVIEW was selected as the development system because of its ease in deploying to multiple target processors, front panel customization capabilities, and parallel architecture. In addition, software was developed in parallel with hardware to accelerate the product development, so software needed to be tested without the hardware in place. Even after the hardware became available, it was critical to test much of the input parameter space (such as extreme voltage readings or simultaneous malfunctions) that is difficult to achieve under normal operating conditions, yet must be tested in practice in order to ensure patient safety.

Approach

To this end, a circuit board (Figure 1) was designed that can be controlled either manually or by a computer to simulate the inputs seen by the sbRIO. It incorporated eight manual toggle switches (with a high impedance drive on one side to allow the computer control option) and five potentiometers. An external power supply allowed for driving at voltages beyond the range that the sbRIO could produce, which is an important part of the parameter space to test. LEDs on the board also provided valuable indicators of the state of the sbRIO and the code running on it.

Development was further accelerated by using a monitor program, developed under LabVIEW that independently accessed the front panel values of the FPGA application on the sbRIO and displayed them on a front panel separate from that of the main VI. The main VI could then be run through its many operations while supplying both normal and abnormal voltage values and digital input combinations with the hardware simulator. The monitor program was used to observe the raw values being measured by the sbRIO to determine that the main VI was taking the correct actions in response to each combination of inputs. LabVIEW's natural parallel processing made the monitor program a straightforward programming task with low cost to the customer but great benefit.

The Figure 1 photograph shows the hardware simulator board in operation. Figure 2 shows the front panel of the monitor program, which closely mimics that of the FPGA portion of the main program. Since it is run in parallel with the main program, the time-consuming task of recompiling the FPGA code with debugging tools does not have to be performed.

Overall, the hardware simulator and the FPGA monitoring program saved Data Science Automation and our customer a large amount of time and money developing this sophisticated, critical component of patient care.

Contact Information

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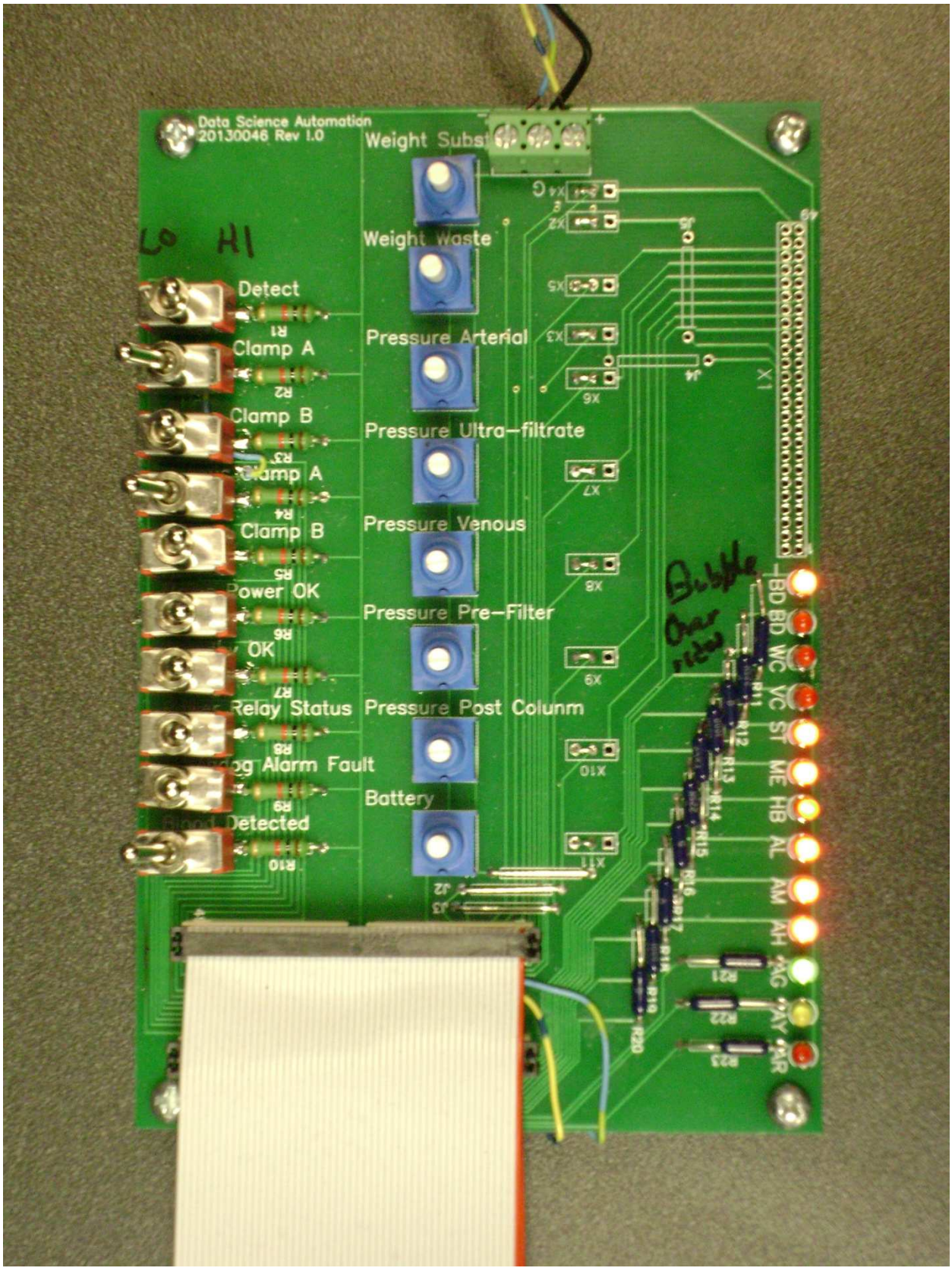

Figure 1 - Photograph of the Hardware Simulator Board

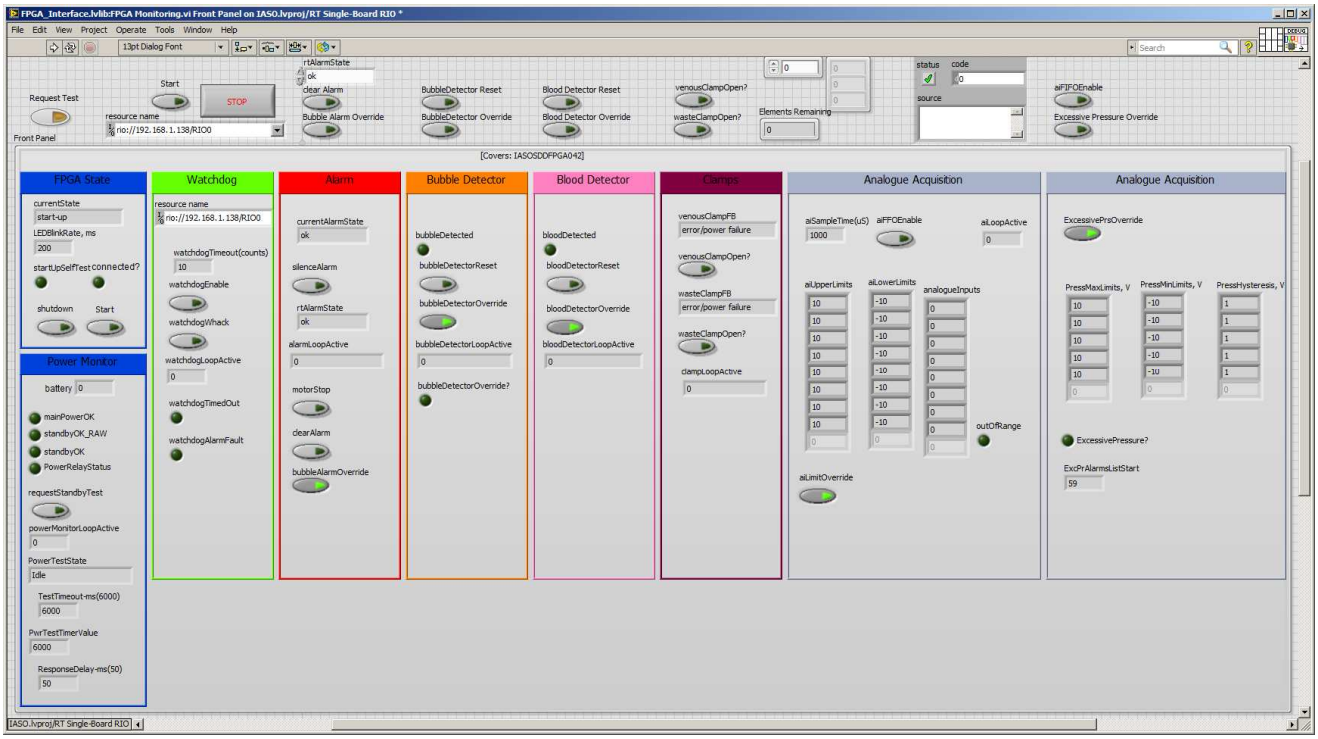

Figure 2 - Front Panel of the FPGA Query Application