



Certified Experts in Automation Engineering to Design, Control, Test & Adapt

500 KVA Variable Frequency Motor Test System

Author(s):

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NI Product(s) Used:

LabVIEW 2012
LabVIEW Real-Time 2012
LabVIEW FPGA
NI cRIO-9082 RT 1.33 GHz Dual-Core Controller, LX150 FPGA with Real-Time OS
NI 9401 (1)
NI 9223 (2)
NI 9220 (1)
NI 9219 (2)
NI 9269 (1)
NI 9155 MXI-Express RIO, LX85 FPGA, 8-slot Chassis
NI 9425 (2)
NI 9476 (2)

Category:

Machine Control
Oil, Gas, and Energy
Transportation, Automotive, and Heavy Equipment

The Challenge

Utilize an FPGA to control insulated-gate bipolar transistors (IGBT) to generate three-phase power for testing various types of motors. In addition the system must perform electrical power measurements replacing typical power monitor instruments that cost tens of thousands of dollars.

The Solution

Data Science Automation leveraged the high-speed of the FPGA and the dual-core processing power of the NI CompactRIO 9082 platform to create a monitoring and control system that converts DC power to kVA AC power over a range of frequencies.

Introduction

Data Science Automation (DSA) is a premier National Instruments (NI) Alliance Partner that specializes in automating and educating the world leading companies. Clients choose DSA because of DSA's deep knowledge of National Instruments products, disciplined process of developing adaptive project solutions, staff of skilled Certified LabVIEW Architects and Certified Professional Instructors, and unique focus on empowerment through education and co-development.

Background

DSA was selected to implement this project for our customer due to our extensive knowledge of the various LabVIEW systems (Windows, Real-Time, and FPGA) and National Instruments hardware. They were attracted to DSA by our standing in the NI Alliance Partner Program and our high number of LabVIEW Architect certifications. A test system of this type had never been completed by our customer and they recognized the complexity of integrating an HMI, RT and FPGA system into a working unit. They first elected to prove the capability of the technology on a smaller scale bench top prototype system before moving into final implementation.

Their legacy systems employed programmable logic controllers (PLC). These PLC units were unable to support the desired new capabilities of the high-speed IGBT power control and power measurements

nor were the PLCs felt to be as adaptable and scalable to their other product lines planned for migration.

Implementation

One of the main goals of the project was to replace power metering instruments that can cost upwards of fifty-thousand dollars each that are used to measure the total harmonic distortion and perform output watt-metering. The main need for the variable frequency output control aspect of the project was to provide capability for motor testing that the end users never had available in prior generations. Larger motors are easier to start using lower frequency power. Being able to vary the frequency from low to high means the test system can safely start larger motors at lower rpm and raise the signal generation frequency to speed the motor up for high speed testing. System safety was also under the protection of the FPGA code since it provides computations and hardware-in-the-loop control at a higher rate than the real-time system. High speed reaction is needed to safely lower the speeds of the motors being tested by engaging power bleed-off brakes to prevent fly-back generated voltage from damaging the test hardware.

The main heart of the system selected was the NI Compact RIO-9082 running a real-time operating system for deterministic measurement and control and dual-core computing power on the embedded device. A touch-panel personal computer running Windows operating system was used to allow operator interaction and test system configuration.

The cRIO-9082 utilized a high-speed digital output card to control the IGBTs for high-speed power generation. Our customer worked with NI to develop an add-on interface card for the NI 9401 high speed digital card for converting the TTL pulses to the higher voltage level necessary for the IGBT control logic cards. The first system prototypes utilized a fixed carrier switching frequency, but the power and speed of the FPGA would certainly allow for variable signal generation carrier frequency if needed in future designs. The software could adapt to future needs without having to select new hardware.

Prior generations of the motor tests system that did not allow for variable frequency testing utilized PLC controllers and large variable resistance coils with physical motor-driven systems that moved contactors up and down the coil packs to generate the necessary energy. The speed of reaction of this system was restricted by the maximum speed of the contactor motors. With the new IGBT technology the system could react nearly instantaneously by varying the PWM signal output to the IGBTs.

The FPGA technology available on the cRIO-9082 allowed for a true parallel programming architecture to be implemented. While the digital control signals to the IGBTs were being generated in one loop on the FPGA the high-speed analog input processing, signal conditioning and scaling was taking place in a parallel loop. The simultaneous sampling, high speed, analog input cards (NI 9223) were able to acquire the voltage and current on the three phase power output of the system simultaneously with six channels measuring Voltage and Current for the three-phase power A, B, C and two expansion channels to be used on future systems. These voltages were scaled to engineering units on the FPGA using the high-throughput math computation provided by NI and passed via DMA to the real-time code for the high-power energy measurements for Vrms, Irms, Phase, leading and lagging information, and total harmonic distortion out to the 31st harmonic.

The power monitoring portion of the code performed on the real-time system had to transfer the data from the FPGA in sizes of 800,000 points (100,000 samples per channel), de-interleave the data into one-dimensional channel arrays and perform all the measurement calculations before the next set of 800,000 points of data was returned from the DMA acquisition.

The following calculations were performed by the system and are what allowed our customer to utilize the FPGA RIO technology to replace the COTS Power Quality Analyzers, saving hundreds of thousands of dollars of hardware and integration costs:

- RMS values and averages of three phases for line-neutral and line-line
 - $V_{A/N \text{ RMS}}$ – Phase A line to neutral voltage RMS [V]
 - $V_{B/N \text{ RMS}}$ - Phase B line to neutral voltage RMS [V]
 - $V_{C/N \text{ RMS}}$ – Phase C line to neutral voltage RMS [V]
 - $V_{A/B \text{ RMS}}$ – Phase A/B line to line voltage RMS [V]
 - $V_{B/C \text{ RMS}}$ - Phase B/C line to line voltage RMS [V]
 - $V_{C/A \text{ RMS}}$ - Phase C/A line to line voltage RMS [V]
 - $V_{\text{AVG RMS}}$ – 3 phase average RMS voltage = $((V_{A/B} + V_{B/C} + V_{C/A}) \div 3)$ [V]
 - $I_{A \text{ RMS}}$ – Phase A RMS current [A]
 - $I_{B \text{ RMS}}$ – Phase B RMS current [A]
 - $I_{C \text{ RMS}}$ – Phase C RMS current [A]
 - $I_{\text{AVG}} = ((I_A + I_B + I_C) / 3)$ – Average of phase RMS currents [A]
- Calculate the Real Power for three phases and total real output power in KW Per phase.
- Calculate Apparent and Reactive Power for three phases and total apparent power in KVA
 - $S_A = V_{A/N \text{ RMS}} * I_{A \text{ RMS}}$ [KVA]
 - $S_B = V_{B/N \text{ RMS}} * I_{B \text{ RMS}}$ [KVA]
 - $S_C = V_{C/N \text{ RMS}} * I_{C \text{ RMS}}$ [KVA]
 - $Q_A = \sqrt{(S_A^2 - P_A^2)}$
 - $Q_B = \sqrt{(S_B^2 - P_B^2)}$
 - $Q_C = \sqrt{(S_C^2 - P_C^2)}$
 - $Q(3\Phi) = Q_A + Q_B + Q_C$
 - $S(3\Phi) = \sqrt{\{[P(3\Phi)]^2 + [Q(3\Phi)]^2\}}$
- Calculate the 3-Phase Power Factor
 - $PF(3\Phi) = P(3\Phi) \div S(3\Phi)$
- Calculate the AC Output Frequency created by the IGBTs to be used for PID control feedback

Independent testing performed by our customer’s engineering staff validated that the metering capabilities of the system exceeded the accuracy and speed of their original power measurement instruments.

Training for the future

In addition to providing the software architecture and integration support, DSA was also able to empower our customer through the use of NI Training classes at our Certified Training Center to educate them on LabVIEW programming. Using Training Memberships, the system engineers attended LabVIEW Core training classes and well as Real-time and FPGA training to give them a solid foundation for understanding and adapting the solution provided.

In addition, DSA also provided custom developer training on the final LabVIEW implementation. This level of training provided insight into the three levels of software architecture – HMI, Real-Time, and FPGA and the interaction mechanisms between them (Figure 1). This allowed our customers to take ownership of the system for support and future adaptations. Their commitment to the Graphical System Design approach was demonstrated by their migration to a Volume License Agreement.

Utilizing their new LabVIEW knowledge our customer was also able to work collaboratively with us on this solution by providing HMI front panel examples. The ease of screen creation and mock up allowed them to present HMI screens to their management for approval at the same time that system development was underway thus shortening the overall system development time.

Conclusion

Data Science Automation was able to leverage the power of the cRIO-9082 to provide our customer with a solution that exceeded their expectations for the power metering and provided them with never before provided system capabilities that they can leverage across multiple future platforms.

The code developed for the variable frequency motor test system can also be reused on future systems that do not require the full hardware and software suite. The modular programming method selected allows for easier sub-system replication and support that will provide lower cost of production and maintenance for their future products.

Contact Information

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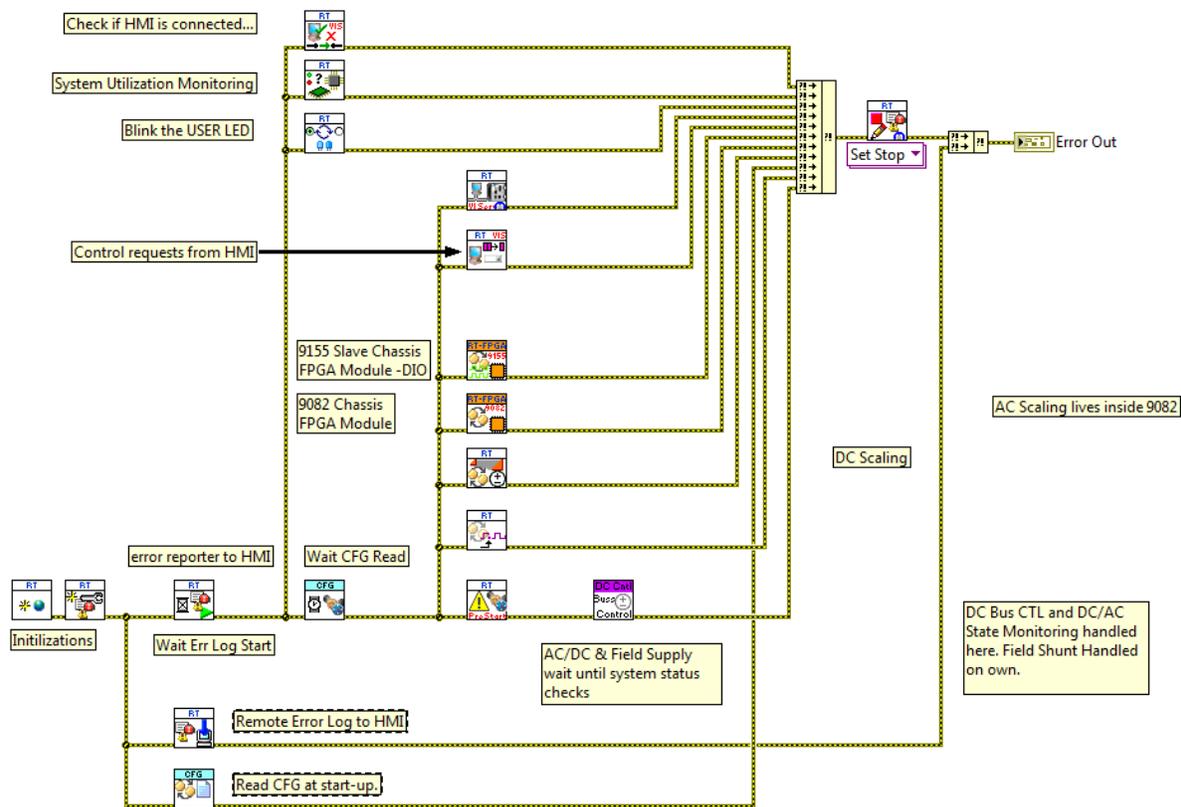


Figure 1. Real-Time Block Diagram Code